PVP 12

Code: EC5T5

III B.Tech - I Semester – Regular Examinations - November 2014

DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Marks: 5x14=70

Answer any **FIVE** questions. All questions carry equal marks

1. a) Discuss the steps in VHDL design flow. 7 M

   b) Explain the use of packages. Give the syntax and structure of a package in VHDL . 7 M

2. a) Explain with example the syntax and function of the following VHDL statements. 7 M
   i) Process statement
   ii) Conditional signal assignment statement
   iii) Loop statement

   b) Explain the various data types supported by VHDL. Give the necessary examples. 7 M

3. a) Explain the sinking and sourcing current in TTL. 7 M

   b) Explain the CMOS gate circuit behavior with resistive load. 7 M

4. a) Draw the logic diagram of 74x151 and explain the operation. 7 M

b) Design a excess-3 to BCD code converter and draw the truth table and logic diagram for it. 7 M

5. a) Design a 16 bit comparator using 74x85 IC's. 7 M

b) Design a two-digit BCD adder with logic gates. Using this logic write the VHDL program in structural style of modeling. 7 M

6. Explain the operation of barrel shifter and write a VHDL program for 16 bit barrel shifter for left and right circular shifts. 14 M

7. a) Explain the function of universal shift register and draw the logic diagram. 7 M

b) Write a VHDL code for a 4 bit counter with enable and clear inputs. 7 M

8. a) With the help of timing waveforms explain the read and write operations of static RAM. 7 M

b) Write a short notes on two dimensional decoding. 7 M